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Abstract
Over the past decades, there were many scholars and engineering immerse themselves in the research of asynchronous VLSI, but most of them only dealt with description, synthesis, and operation of asynchronous controller. Surprisingly, only a few literature did discuss the implementation of the self-timed datapath. Therefore, this thesis aims on the low-power design, and by the aspect of achieving power saving, the same methodology is adopted to assist engineers to implement highly-efficient self-timed datapath components.
This work present a design methodology to implement low-power CMOS digital circuit based on pseudo-DCVSL architecture, of which the function block is bundled by an auxiliary circuit. In which implementation, the completion of the realized complement depends on two situations: the worse-case matched delay time and the output transition of the target logic function. The advantage of the auxiliary circuit is a few transistors are needed but it does improve the performance of the circuit significantly.
We undergo TSMC 0.35um process for the post-layout simulation and verification of the architecture. For single-stage designs, it consumes 15% less power than other conventional dynamic architectures, saves up to 15% of layout area, and enhances up to 15% of the average delay time. In the case of 4-bit self-timed carry-chain structure, the result we obtained through the simulation shows an improvement of 35%, 40%, and 20% with respect to power, area, and delay. Therefore, we could infer that the improvement will be much conspicuous for larger designs.
Moreover, the proposed pseudo-DCVSL structure include an additional feature of delay fault recovery. After we conduct a post-layout simulation, the result shows that there is approximately 400ps of extra safety marginal time provided by the auxiliary circuit. Therefore, when the mapped delayed time is insufficient, the structured circuit could automatically adjust the error signal to its correct value. The comprehensive post-layout simulation result shows that proposed pseudo-DCVSL structure is not merely a high-efficient self-timed circuit on the implementation of a small size circuit, but the same structure will outperform in the mid-size or larger size of circuits when the circuits get much more complexed.
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